

## METHOD FOR DESIGN VALIDATION OF COMPLEX IC

### Abstract of the Disclosure

5 A method for design validation of complex IC with use of  
a combination of electronic design automation (EDA) tools and  
a design test station at high speed and low cost. The EDA  
tools and device simulator are linked to the event based test  
system to execute the original design simulation vectors and  
testbench and make modifications in the testbench and event  
based test vectors until satisfactory results are obtained.  
10 Because EDA tools are linked with the event based test  
system, these modifications are captured to generate a final  
testbench that provides satisfactory results.

15

20

SPC-AD31.003  
082701